CLAIMS

What is claimed is:

1. A digital timing synchronizer of a receiver for timing synchronization to a transmitter in a wireless communication system, wherein the received signal has a timing error with respect to a reference code, comprising:

a channel estimator configured for estimating an initial code phase of the received signal;

a code generator configured to generate a timing reference code that is adjustable by integer increments; and

an interpolation feedback circuit configured for interpolation and correction of the timing error, whereby the interpolation is achieved through an integer code shift, plus a quantized fractional delay estimate selected from a look-up table of quantized fractional delay estimate values and their associated predetermined interpolator coefficients, from which a time corrected version of the received signal is produced.

2. The invention of claim 1 wherein the interpolation feedback circuit further comprises:

an interpolator normalized to a sampling rate, configured to shift the received signal in time by a fractional delay or advancement;

a timing error estimator for determining timing error estimate based on timing difference between an output signal of the interpolation feedback circuit and the timing reference code;

an interpolator controller responsive to the timing error estimate for producing and sending an integer code shift signal to the code generator in a direction opposite of the timing error estimate, producing a fractional delay estimate within a predetermined range for determining interpolation coefficients; and

a quantizer having the look-up table with stored interpolator coefficients associated with predetermined quantized fractional delay estimate values, configured

to select from the look-up table a quantized fractional delay estimate closest in value to the fractional delay estimate.

3. The invention of claim 2, wherein the interpolation feedback circuit further comprises a filter for filtering the timing error estimate to produce a delay estimate value with a sign opposite that of the timing error estimate, whereby the interpolator controller regulates the delay estimate within a predetermined operating range related to the timing error estimator configuration.

4. The invention of claim 3 wherein the interpolation feedback circuit further comprises a down-sampler responsive to the interpolator controller, configured to reduce the sampling rate of the received signal by an over-sampling factor and according to a base point related to the ratio of sampling rate of the received signal and the delay estimate.

5. The invention of claim 2 wherein the interpolator is an MMSE optimized FIR interpolator.

6. The invention of claim 1, wherein the received signal comprises multiple paths and the interpolation feedback circuit further comprises a post processing unit configured to process the estimated initial code phase and to estimate signal and noise power against a noise threshold, thereby producing an initial code phase to which the code generator develops the reference code.

7. The invention of claim 1 wherein the predetermined range for the fractional delay estimate is between (–1) and (1).

8. The invention of claim 1 wherein the received signal is over-sampled by a factor of L and the predetermined number of quantized fractional adjustment values is

Q/L number of quantization levels, determined according to the desired timing accuracy T/Q for timing adjustment, where T represents the sampling period, Q represents a positive integer, and L is a positive integer.

9. A receiver including the digital timing synchronizer according to claim 1.

10. A wireless transmit/receive unit including the digital timing synchronizer according to claim 1.

11. A method for digital timing synchronization of a receiver to a transmitter in a wireless communication system, wherein the received signal has a timing error with respect to a reference code, comprising:

estimating an initial code phase of the received signal;

generating a timing reference code that is adjustable by integer increments; and

interpolating and correcting the timing error, whereby the interpolating is achieved through an integer code shift, plus a quantized fractional delay selected from a look-up table of quantized fractional delay values and their associated predetermined interpolator coefficients, from which a time corrected version of the received signal is produced.

12. The method of claim 11 wherein the interpolating and correcting step further comprises:

shifting the received signal in time by a fractional delay or advancement;

determining a timing error estimate based on a timing difference between the time corrected version of the received signal and the timing reference code;

producing an integer code shift signal in a direction opposite of the timing error estimate;

producing a fractional delay estimate within a predetermined range for determining interpolation coefficients;

storing, in a look-up table, predetermined quantized fractional delay estimate values associated interpolator coefficients; and

selecting, from the look-up table, a quantized fractional delay estimate closest in value to the fractional delay estimate.

13. The method of claim 12, wherein the interpolating step further comprises filtering the timing error estimate to produce a delay estimate value with a sign opposite that of the timing error estimate, whereby the delay estimate is regulated within a predetermined operating range related to the timing error estimator configuration.

14. The method of claim 13 wherein the interpolating step further comprises reducing the sampling rate of the received signal by an over-sampling factor, according to a base point related to the ratio of sampling rate of the received signal and the delay estimate.

15. The method of claim 11, wherein the received signal comprises multiple paths and the interpolating step further comprises processing the estimated initial code phase and estimating signal and noise power against a noise threshold, thereby producing an initial code phase to which the code generator develops the reference code.

16. The method of claim 12 wherein the predetermined range for the fractional delay estimate is between (–1) and (1).